REMARKS

Claims 1-27 are pending. The Examiner rejected claims 1-27 including independent claims 1, 11, and 21 under 35 U.S.C. 120(e) as being anticipated by Oh (6,996,016 B2). The Examiner also rejected claims 1-7, 11-17, and 21-27 under 35 U.S.C. 102(e) as being anticipated by Wingard (6,725,313). Neither Oh nor Wingard are believed to teach or suggest all of the elements of the claims. However, to facilitate prosecution, the independent claims have been amended to recite "providing a selection mechanism to a user to have the primary component access the secondary component using fixed latency or variable latency and receiving a selection from the user to have the primary component issue a plurality of reads to the secondary component using variable latency." This amendment is supported on pages (page 6, line 31 – page 7, line 13), Figure 6, and associated description.

Neither Oh nor Wingard teach or suggest "providing a selection mechanism to a user" or "receiving a selection from a user to have the primary component issue a plurality of reads to the secondary component using variable latency."

Oh notes "the system bus 106 comprises a bi-directional line 114 (shown in phantom) that transmits a WAIT_DQS signal and a plurality unidirectional transmission lines propagating conventional control and command signals. Such conventional control and command signals comprise, among other such signals, a Clock (CLK) signal, an Address (e.g., 21-bit address word A20-A0) signal, an Address Valid (ADV) signal, a Write Enable (WE) signal, and a Chip Select (CS) signal (all discussed below in reference to FIGS. 3-7)." (column 4, lines 12-24)

Wingard describes a communications systems using multilevel connection identification. "System 1000 includes initiator functional block 1002, which is connected to initiator interface module 1004 by interconnect 1010. Initiator interface module 1004 is connected to target interface module 1006 by shared communications bus 1012. Target interface module 1006 is connected to target functional block 1008 by an interconnect 1010. Typically, shared communications bus 1012 is analogous to shared communications bus 112 of FIG. 1 or to shared communications bus 114 of FIG. 1." (description of Figure 4)

The Examiner relies on Oh to teach the elements of the claims. It is acknowledged that Figure 1 and the corresponding text do describe a processor 110 and a memory 104 and buses 106 and 108. However, Oh is not believed to teach or suggest receiving information about the primary component and the second component and generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components. Oh is also believed not to teach "providing a selection mechanism to a user" or "receiving a selection from a user to have the primary component issue a plurality of reads to the secondary component using variable latency."

The Examiner may attempt to argue that receiving this information and generating the interconnection module are inherent in Oh. The Applicants respectfully disagree. The interconnection module in Oh may be standard bus used to connect components. No interconnection module has to be generated. In many instances, a standard bus is used as an interconnect. However, the techniques of the present invention recite "receiving information about a primary component and a secondary component" and "generating an interconnection module coupling the primary component to the secondary component." Oh does not teach or suggest any receiving information about a first primary component or receiving any information about a first secondary component. Oh furthermore does not teach or suggest "generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components."

The Examiner argues that receiving information ... and generating an interconnection module is inherent. The Applicants respectfully disagree. Primary and secondary components along with buses may be selected and placed without any "receiving information... and generating an interconnection module." Many conventional implementations including Oh, it is believed, use this approach.

Claim 11 recites an input interface configured to receive information associated with a primary component and information associated with a secondary component ... and a processor configured to generate interconnection circuitry coupling the primary component to

the secondary component, the interconnection module including data, address, and control lines for the programmable chip. Oh does not teach or suggest an input interface or any processor configured to perform the above noted elements. Oh only describes a processor connected to a memory over a bus.

The Examiner also relies on Wingard to teach the elements of the claims. Although Wingard shows a master and a slave along with connection lines, Wingard does not teach or suggest "generating interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module support a system having both fixed and variable latency components" or "receiving information ... and generating an interconnection module." Again, generating an interconnection module or interconnection circuitry is not inherent. As noted above, primary and secondary components along with buses may be selected and placed without any "receiving information... and generating an interconnection module." Many conventional implementations including Wingard, it is believed, use this approach.

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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